Sub A8

ABSTRACT OF THE DISCLOSURE

An interface for transferring data between a central processing unit (CPU) and a plurality of coprocessors is provided. The interface includes an instruction bus and a data bus. The instruction bus is configured to transfer instructions to the plurality of coprocessors in an instruction transfer order, where particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the CPU. The data bus is configured to subsequently transfer the data. Data order signals within the data bus prescribe a data transfer order that differs from the instruction transfer order by prescribing a transfer corresponding to a specific outstanding particular instruction relative to all outstanding particular instructions.